Item	Location	Feature description	Notes
1	J34	Front I/O header	Table 1
2	J27	Internal speaker	Table 2
3	J28	Single-Port USB 2.0 Header	Table 3
4	J32	Single-Port USB 2.0 Header	Table 3
5	J36	Single-Port USB 2.0 Header	Table 3
6	J2J	Dual-Port USB 2.0 Header	Table 4
7	J12	CPU FAN header	Table 5
8	J13	Front FAN header	Table 6
9	J7	LVDS power 1x3 pin header	Table 7
10	J8	LVDS inverter board header	Table 8
11	J5	LVDS header	Table 9
12	J10	RJ45 LED behavior	Table 10
13	J2	CMOS Clear	Table 11

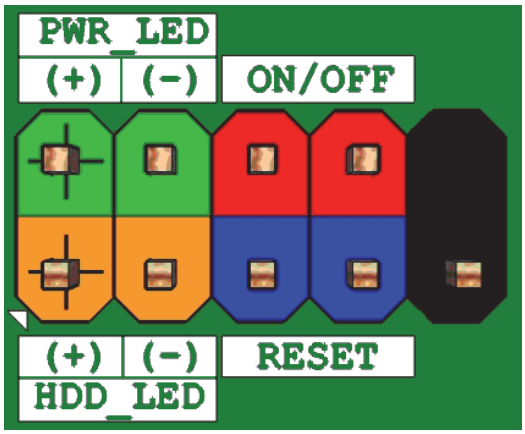


Figure 1 Front panel main header pin-out

Pin	Signal Name	Description	Pin	Signal Name	Description
1	HDD_POWER_LED	Pull-up resistor (750 ·) to +5V	2	POWER_LED_MAIN	[Out] Front panel LED (main color)
3	HDD_LED#	[Out] Hard disk activity LED	4	POWER_LED_ALT	[Out] Front panel LED (alt color)
5	GROUND	Ground	6	POWER_SWITCH#	[In] Power switch
7	RESET_SWITCH#	[In] Reset switch	8	GROUND	Ground
9	+5V_DC	Power	10	KEY	No pin

Table 1 Front panel main header signals

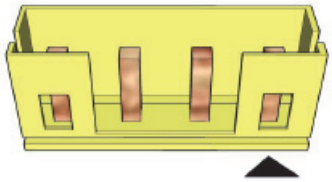


Figure 2 Internal speaker

Pin	Signal Name
1	Front_L-
2	Front_L+
3	Front_R+
4	Front_R-

Table 2 Internal header signals

Figure 3 Front panel USB header pin-out

Pin	Signal name
1	+5V DC
2	Data (negative)
3	Data (positive)
4	Ground
5	Key (no pin)

Table3 Front panel USB header

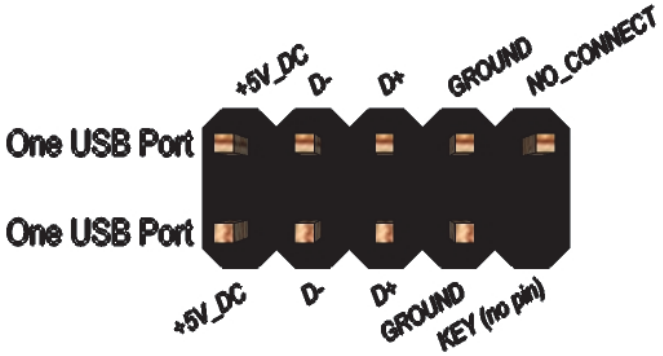


Figure 4 Front panel USB header pin-out

Pin	Signal	Pin	Signal
1	+5V DC	2	+5V DC
3	Data (negative)	4	Data (negative)
5	Data (positive)	6	Data (positive)
7	Ground	8	Ground
9	Key (no pin)	10	No Connect

Table 41 Front panel USB header signals

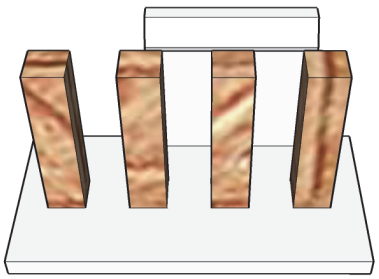


Figure 5: Processor fan header

Pin	Signal
4	FAN_CTRL
3	FAN_TACH
2	VCC-12V
1	GND

Table 5: Processor fan header

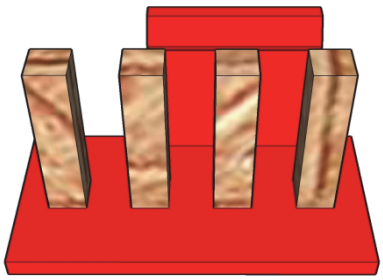


Figure 6: System fan header

Pin	Signal
4	FAN_CTRL
3	FAN_TACH
2	VCC-12V
1	GND

Table 6: Processor fan header

Pins 1&2: jumper position for 12V

Pins 2&3: jumper position for 19V

Pin	Signal Name
1	12V
2	BKLT_PWR
3	19V

Table 7: Inverter power voltage selection header

Figure 8: LVDS inverter power header

Pin	Signal Name	Description
1	BKLT_EN	Backlight enable
2	BKLT_PWM	Backlight PWM control
3	12V/19V	Inverter power
4	12V/19V	Inverter power
5	GND	Ground
6	GND	Ground
7	BRIGHTNESS_UP	BRIGHTNESS UP
8	BRIGHTNESS_DOWN	BRIGHTNESS DOWN

Table 8: 8-pin LVDS inverter power header pin-out reference

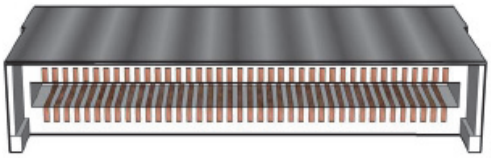


Figure 9: LVDS data header

Pin	Signal	Description
1	LA_DATAP3	LVDS Channel A diff data output - positive
2	LA_DATAN3	LVDS Channel A diff data output - negative
3	LA_DATAP2	LVDS Channel A diff data output - positive
4	LA_DATAN2	LVDS Channel A diff data output - negative
5	LA_DATAP1	LVDS Channel A diff data output - positive
6	LA_DATAN1	LVDS Channel A diff data output - negative
7	LA_DATAP0	LVDS Channel A diff data output - positive
8	LA_DATAN0	LVDS Channel A diff data output - negative
9	LB_DATAP3	LVDS Channel B diff data output-positive
10	LB_DATAN3	LVDS Channel B diff data output-negative
11	LB_DATAP2	LVDS Channel B diff data output-positive
12	LB_DATAN2	LVDS Channel B diff data output-negative
13	LB_DATAP1	LVDS Channel B diff data output-positive
14	LB_DATAN1	LVDS Channel B diff data output-negative
15	LB_DATAP0	LVDS Channel B diff data output-positive
16	LB_DATAN0	LVDS Channel B diff data output-negative
17	GND	Ground
18	3.3V/5V/12V	Selectable LCD power output
19	3.3V/5V/12V	Selectable LCD power output
20	3.3V/5V/12V	Selectable LCD power output
21	NC	NC
22	EDID_3.3V	VCC3
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	LA_CLKP	LVDS Channel A diff data output - positive
27	LA_CLKN	LVDS Channel A diff data output - negative
28	GND	Ground
29	GND	Ground
30	GND	Ground

31	EDID_CLK	EDID/DDC clock signal
32	BKLT_EN	
33	BKLT_CTRL	
34	LB_CLKP	LVDS Channel B diff data output - positive
35	LB_CLKN	LVDS Channel B diff data output - negative
36	BKLT_PWR	Selectable BKLT power output
37	BKLT_PWR	Selectable BKLT power output
38	BKLT_PWR	Selectable BKLT power output
39	NC	NC
40	EDID_DATA	EDID/DDC data signal

Table 9: 40-pin LVDS data header pin-out reference

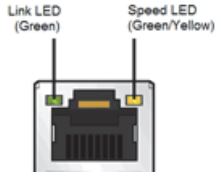
Diagram	LED	Color	State	Condition
	Link	N/A	Off	LAN link is not established
		Green	On	LAN link is established
			Blinking	LAN activity occurring
	Speed	N/A	Off	10 Mb/s data rate
		Green	On	100 Mb/s data rate
		Yellow	On	1000 Mb/s data rate

Table 10: RJ45 LED behavior

Note: LAN solution must be tested for IEEE802.3 conformance.

CMOS Clear

1-2	Clear CMOS
2-3	Normal

Table 11: CMOS Clear behavior